What is Claimed is:

1. A supply voltage detection circuit for an input/output terminal of an integrated circuit device, comprising:

a first voltage detection circuit having an input for receiving a first supply voltage signal and an output for providing a first detection signal that indicates when the voltage level of the first supply voltage signal is below a first steady state supply level;

a second voltage detection circuit having an input for receiving a second supply voltage signal and an output for providing a second detection signal that indicates when the voltage level of the second supply voltage signal is below a second steady state supply level; and

a logic circuit for receiving the first and second detection signals and providing at least one detected condition signal for disabling current flow through the input/output terminal when either the first supply voltage signal is below the first steady state supply level or the second supply voltage signal is below the second steady state supply level.

2. The detection circuit of claim 1 further comprising a bias circuit for receiving the first supply voltage signal and a signal corresponding to the voltage at the input/output terminal, the bias circuit providing a bias power voltage signal substantially equal to the greater of the first supply voltage signal and the voltage at the input/output terminal.

3. The detection circuit of claim 2 wherein the first voltage detection circuit is powered by the bias power voltage signal.

4. The detection circuit of claim 3 wherein the first steady state supply level is greater than or equal to the second steady state supply level, and the second voltage detection circuit is powered by the first supply voltage signal.

5. The detection circuit of claim 3 wherein the first steady state supply level is greater than or equal to the second steady state supply level, and the second voltage detection circuit is powered by the bias power voltage signal.

6. The detection circuit of claim 3 wherein the first supply voltage signal is provided by an input/output power supply and the second supply voltage signal is provided by a core power supply.

7. The detection circuit of claim 6 wherein the first steady state supply level is substantially between 1.6 V and 3.3 Volts and the second steady state supply level is substantially equal to 1.5 V.

8. The detection circuit of claim 6 in combination with an input/output buffer circuit for the input/output terminal, the input/output buffer circuit being powered by the bias power voltage signal and receiving the at least one detected condition signal.

9. The detection circuit of claim 1 wherein each of the first and second voltage detection circuits comprises:

a first latch having an input and an output, the output of said voltage detection circuit being at the input of the first latch;

a first transistor coupled between the input of said voltage detection circuit and the output of the first latch, the first transistor having a control terminal coupled to a node for a power signal for said voltage detection circuit; and

a second transistor coupled between a reference supply voltage and the input of the first latch, the second transistor having a control terminal coupled to the input of said voltage detection circuit.

10. The detection circuit of claim 9 wherein the first transistor has a lower conductivity than the second transistor.

11. The detection circuit of claim 10 wherein the first steady state supply level is greater than or equal to the second steady state supply level, the power signal for the first voltage detection circuit is the greater of the first supply voltage signal and a signal corresponding to the voltage at the input/output terminal, and the power signal for the second voltage detection circuit is the first supply voltage signal.

12. The detection circuit of claim 10 wherein the first steady state supply level is greater than or equal to the second steady state supply level, and the power signal for each of the first and second voltage detection circuits is the greater of the first supply voltage signal and a signal corresponding to the voltage at the input/output terminal.

13. The detection circuit of claim 10 wherein

the first transistor is an NMOS transistor having a source terminal coupled to the input of said voltage detection circuit, a drain terminal coupled to the output of the first latch, and a gate terminal coupled to the power signal node for said voltage detection circuit; and

the second transistor is an NMOS transistor having a source terminal coupled to the reference supply voltage, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the input of said voltage detection circuit.

14. The detection circuit of claim 10 wherein the first latch is a half latch comprising:

an inverter having an input and an output, the input of the inverter being the input of the first latch and the output of the inverter being the output of the first latch; and

a third transistor coupled between the input of the first latch and the power signal node for said voltage detection circuit, the third transistor having a control terminal coupled to the output of the first latch.

15. The detection circuit of claim 14 wherein each of the first and second voltage detection circuits includes a second half latch comprising:

a second inverter having an input and an output, the input of the second inverter being coupled to the input of the first latch;

a fourth transistor coupled between the input of the first latch and the power signal node for said voltage detection circuit, the third transistor having a control terminal coupled to the output of the second inverter.

16. The detection circuit of claim 15 wherein

the third transistor is a PMOS transistor having a source terminal coupled to the power signal node for said voltage detection circuit, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the output of the first latch; and

the fourth transistor is a PMOS transistor having a source terminal coupled to the power signal node for said voltage detection circuit, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the output of the second inverter.

17. The detection circuit of claim 1 wherein the logic circuit comprises a NOR gate having a first input for receiving the first detection signal and a second input for receiving the second detection signal, and wherein the logic circuit generates a pair of complementary detected condition signals.

18. The detection circuit of claim 1 wherein the integrated circuit is fabricated using CMOS technology.

19. The detection circuit of claim 1 wherein the integrated circuit device is a programmable logic device.

20. An integrated circuit device comprising:

a plurality of terminals including

a first power terminal for receiving an input/output supply voltage signal,

a second power terminal for receiving a core supply voltage signal, and

one or more input/output terminals for receiving input signals to the device or delivering output signals from the device,

for each input/output terminal, a supply voltage detection circuit comprising

a first voltage detection circuit having an input for receiving the input/output supply voltage signal and an output for providing a first detection signal that indicates when the level of the input/output supply voltage signal is below a steady state input/output supply level;

a second voltage detection circuit having an input for receiving the core supply voltage signal and an output for providing a second detection signal that

indicates when the level of the core supply voltage signal is below a steady state core supply level; and

a logic circuit for receiving the first and second detection signals and providing at least one detected condition signal for disabling current flow through the input or the output terminal when either the input/output supply voltage signal is below the steady state input/output supply level or the core supply voltage signal is below the steady state core supply level.

21. The integrated circuit device of claim 20 further comprising: for each input/output terminal, an input/output buffer circuit connected to said input terminal and receiving the at least one detected condition signal from the detection circuit corresponding to said input/output terminal.

22. The integrated circuit device of claim 20 wherein each supply voltage detection circuit further comprises a bias circuit for receiving the input/output supply voltage signal and a signal corresponding to the voltage at the corresponding input or output terminal, the bias circuit providing a bias power voltage signal substantially equal to the greater of the input/output supply voltage signal and the voltage at the corresponding input or output terminal.

23. The integrated circuit device of claim 22 wherein the steady state input/output supply level is greater than or equal to the steady state core supply level and, in each supply voltage detection circuit, the first voltage detection circuit is powered by the bias power voltage signal and the second voltage detection circuit is powered by the input/output supply voltage signal.

24. The integrated circuit device of claim 23 wherein the steady state input/output supply level is substantially between 1.6 V and 3.3 Volts and the steady state core supply level is substantially equal to 1.5 V.

25. The integrated circuit device of claim 20 wherein, in each of the supply voltage detection circuits, each of the first and second voltage detection circuits comprises:

a first latch having an input and an output, the output of said voltage detection circuit being at the input of the first latch;

a first transistor coupled between the input of said voltage detection circuit and the output of the first latch, the first transistor having a control terminal coupled to a node for a power signal for said voltage detection circuit; and

a second transistor coupled between a reference supply voltage and the input of the first latch, the second transistor having a control terminal coupled to the input of said voltage detection circuit.

26. The integrated circuit device of claim 25 wherein, in each of the first and second voltage detection circuits in each of the detection circuits, the first transistor has a lower conductivity than the second transistor.

27. The detection circuit of claim 20 wherein the integrated circuit device is a programmable logic device.

28. A supply voltage detection circuit for an input/output terminal of an integrated circuit device, comprising:

a first power terminal for receiving a first supply voltage signal;

a second power terminal for receiving a second supply voltage signal;

a first voltage detection circuit having an input coupled to the first power terminal and an output providing a first detection signal that indicates when the voltage level of the first supply voltage signal is below a first steady state supply level;

a second voltage detection circuit having an input coupled to the second power terminal and an output providing a second detection signal that indicates when the voltage level of the second supply voltage signal is below a second steady state supply level; and

a logic circuit having first and second inputs coupled respectively to the outputs of the first and second voltage detection circuits, the logic circuit having at least one output providing at least one detected condition signal that disables current flow through

the input/output terminal when either the first supply voltage signal is below the first steady state supply level or the second supply voltage signal is below the second steady state supply level.

29. The detection circuit of claim 28 further comprising a bias circuit having a first input coupled to the first power terminal and a second input coupled to the input/output terminal, the bias circuit having an output providing a bias power voltage signal that is substantially equal to the greater of the first supply voltage signal and the voltage at the input/output terminal.

30 The detection circuit of claim 29 wherein the first voltage detection circuit has a power input coupled to the output of the bias circuit.

31. The detection circuit of claim 30 wherein the first steady state supply level is greater than or equal to the second steady state supply level, and the second voltage detection circuit has a power input coupled to the first power terminal.

32. The detection circuit of claim 30 wherein the first supply voltage signal is provided by an input/output power supply coupled to the first power terminal, and the second supply voltage signal is provided by a core power supply coupled to the second power terminal.

33. The detection circuit of claim 32 wherein the first steady state supply level is substantially between 1.6 V and 3.3 V and the second steady state supply level is substantially equal to 1.5 V.

34. A method of detecting a supply voltage condition for an input/output terminal of an integrated circuit device, comprising:

providing a first detection signal that indicates when the voltage level of a first supply voltage signal is below a first steady state supply level;

providing a second detection signal that indicates when the voltage level of a second supply voltage signal is below a second steady state supply level; and

combining the first and second detection signals to provide at least one detected condition signal for disabling current flow through the input/output terminal when either the first supply voltage signal is below the first steady state supply level or the second supply voltage signal is below the second steady state supply level.

35. The method of claim 34 further comprising:

providing a bias power voltage signal substantially equal to the greater of the first supply voltage signal and the voltage at the input/output terminal;

powering a circuit for providing the first detection signal with the bias power voltage signal; and

powering a circuit for providing the second detection signal with the first supply voltage signal.

36. The method of claim 35 wherein the first supply voltage signal is an input/output power supply signal and the second supply voltage is a core power supply signal.

37. The method of claim 34 further comprising providing the at least one detected condition signal to an input/output buffer circuit for the input/output terminal.